1: Use DeMorgan’s Law to find the inverse of these logic functions:

\[ Y = \overline{A} + BC + \overline{A} \overline{B} \overline{D} \]

\[ Y = (A+C)(\overline{B}+C)(\overline{A}+C+D) \]

\[ Y = AB + \overline{C}D + A\overline{BCD} \]

2: In the circuit below, draw a timing diagram which illustrates a possible timing glitch:

![Timing Diagram](image)

3: Write a logic expression for a 3:1 MUX.

4: How many 2:1 MUXes does it take to build a 15:1 MUX?

5: Draw the Karnaugh maps for a 2-bit subtract circuit (Subtracts any of the numbers 0,1,2,3 from any of the numbers 0,1,2,3). Assume any negative numbers are “don’t care” cases.

6: If the circuit in problem 5 instead returns all zeros, does the logic become more or less complex?