1: Use DeMorgan’s Law to find the inverse of these logic functions:

\[ Y = \overline{A} + BC + \overline{A}\overline{B}\overline{C}\overline{D} \]

\[ Y = (A+C)(\overline{B}+\overline{C})(A+C+\overline{D}) \]

\[ Y = \overline{A}\overline{B} + \overline{C}D + \overline{A}B\overline{D} \]

2: Write a logic expression for a 5:1 MUX.

3: How many 2:1 MUXes does it take to build a 15:1 MUX?

4: Draw the Karnaugh maps for a 2-bit subtract circuit (Subtracts any of the numbers 0,1,2,3 from any of the numbers 0,1,2,3). Assume any negative numbers are “don’t care” cases.

5: If the circuit in problem 5 instead returns all zeros, does the logic become more or less complex?

6: Write verilog code that describes a 1:4 demultiplexer as a single module.