Design a string Reverse whose output will be True if input value

(1) Draw state diagram
(2) Implement solution as a module in

Verilog
Design a circuit that takes in a bitstream and outputs 1 if the number of 1's is a multiple of 3, and 0 otherwise.
Fill out the following timing diagram assuming that each vertical line represents a single gate delay.
If reset = 1, Q = 0.
What will Q do based on the information known?
Use De Morgan's to simplify

\[ f = \overline{\overline{a+d} \cdot \overline{b+c} \cdot \overline{a+b}} \]
Draw the circuit diagram for the following boolean equation using only NAND, NOR, and inverter gates. Use the smallest number of gates possible.

\[ F = AB + (\overline{A+B+C}) + \overline{AB\overline{C}} \]
Create the circuit diagrams and the truth tables

\[ F = XYZ \overline{Z} + XYZ + \overline{Z} \oplus Y \]
Write down **ALL** the correct answers of the minimum Sum of Products equation of the following K-Map.
EE271

Homework 3A

P)

Design a circuit that takes 4 bit inputs $A_3 A_2 A_1 A_0$ and gives two outputs $out_1$ and $out_2$. The $out_1$ is true if and only if $A_1 A_0$ are equal and $A_2$, $A_3$ are not equal. The $out_2$ is true if and only if $A_1 A_0$ is even and $A_3 A_2$ is odd. When all inputs are false or true, outputs do not matter. Draw your circuit with minimum numbers of gats as possible. You can use a truth table, and k-map to produce a simplified Sum-of-Products equation for the circuit.
A lottery machine that have four output that only when three or more of them are true buyers can have reward. Using k-map to produce a simplified Sum-of-Products equation. Draw the corresponding circuit diagram.
Implement the following FSM.