If reset = 1, Q = 0. What will Q do based on the Information Known?

always. If @ (posedge clk) begin
if (reset)
  Q <= 0;
else
  Q <= D;
end
Design a circuit that takes in a bitstream and outputs 1 if the number of 1's is a multiple of 3, including the current input, and 0 otherwise.
Fill out the following timing diagram assuming that each vertical line represents a single gate delay.
Write down **ALL** the correct answers of the minimum Sum of Products equation of the following K-Map.

\[ F = AC + \overline{AC} + \overline{A}BD = \overline{A} + C + ABD \]

\[ AC + \overline{AC} + \overline{BCD} = \overline{A} + C + BCD \]

\[ B(C + D) \leq \text{Product of Sum} \]
Use De Morgan's to simplify

\[ f = \overline{a+d} \cdot \overline{b+c} \cdot \overline{a+b} \]

\[ = (a+d) + (\overline{b+c}) + (\overline{a+b}) \]

\[ = (a+d) + (\overline{b} + \overline{c}) + (\overline{a} + \overline{b}) \]

\[ = a + \overline{b} + c + d \]

Does \( \overline{a+b} + a \overline{b} = 1 \)
Draw the circuit diagram for the following Boolean equation using only NAND, NOR, and inverter gates. Use the smallest number of gates possible.

\[ F = AB + (A + B + C) + \overline{A} \overline{B} \overline{C} \]

\[ = AB + \overline{AB} \overline{C} + \overline{A} \overline{B} \overline{C} \]

\[ = AB + \overline{AB} \]

![Circuit Diagram](image)