Review Problem 27

- Draw the circuit diagram for this code

```verilog
module foo (clk, reset, in, out);
    input logic clk, reset, in;
    output logic out;
    enum { A=0, B=1 } ps, ns;

    always_comb begin
        case (ps)
            A: ns = B;
            B: if (in) ns = B;
                else ns = A;
        endcase
        out = ~ps;
    end

    always_ff @(posedge clk) begin
        if (reset) ps <= A;
        else ps <= ns;
    end
endmodule
```

```
<table>
<thead>
<tr>
<th>PS</th>
<th>IN</th>
<th>Out</th>
<th>NS</th>
<th>NS</th>
<th>PS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
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</table>
```

\[ NS = \overline{PS} + \overline{IN} \]

\[ \text{out} = \overline{PS} \]
FSM Word Problem: Traffic Light Controller

A busy highway is intersected by a little used farmroad. Detectors sense the presence of cars waiting on the farmroad. With no car on farmroad, lights remain green in highway direction. If vehicle on farmroad, highway lights go from Green to Yellow to Red, allowing the farmroad lights to become green. These stay green only as long as a farmroad car is detected but never longer than a set interval. When these are met, farm lights transition from Green to Yellow to Red, allowing highway to return to green. Even if farmroad vehicles are waiting, highway gets at least a set interval as green.

Assume you have an interval timer that generates a short time pulse (TS) and a long time pulse (TL) in response to a set (ST) signal. TS is to be used for timing yellow lights and TL for green lights.
Traffic Light Controller (cont.)

Picture of Highway/Farmroad Intersection:
Traffic Light Controller (cont.)

- Tabulation of Inputs and Outputs:

<table>
<thead>
<tr>
<th>Input Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>reset</td>
<td>place FSM in initial state</td>
</tr>
<tr>
<td>C</td>
<td>detect vehicle on farmroad</td>
</tr>
<tr>
<td>TS</td>
<td>short time interval expired</td>
</tr>
<tr>
<td>TL</td>
<td>long time interval expired</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HG, HY, HR</td>
<td>assert green/yellow/red highway lights</td>
</tr>
<tr>
<td>FG, FY, FR</td>
<td>assert green/yellow/red farmroad lights</td>
</tr>
<tr>
<td>ST</td>
<td>start timing a short or long interval</td>
</tr>
</tbody>
</table>
Traffic Light Controller (cont.)

- State Diagram

- Reset

- TL+ E/HG, FR

- HG 00

- TS/HG, FR, ST

- HY 01

- TS/HY, FR

- FY 11

- TS/FY, HR

- TL+ C/FY, HR, ST

- FG 10

- C* TL/FG, HR