Practical Considerations - Introduction to Signal Behaviour in the Real World

Overview
In this lesson we will
✓ Will take first steps into real-world
✓ Examine a high-level view of and lay foundation for study of digital signaling and
  signal quality
✓ Introduce some related concepts and vocabulary
✓ Introduce and examine basic issues affecting digital signal quality
✓ Move into advanced area called signal integrity

Introduction
In text book or ideal world
Signals change state or propagate though combinational or sequential networks
In zero time

As we take first steps into real world
Begin to see that textbook models
Do not exactly match what we see on lab bench
Begin to see that quality or integrity of textbook signals
Different from we see in our circuits

Signal edges and transitions
Not as crisp
We see oscillations called ringing as signals change state

Signal propagation
Meander to destination
Potentially take different routes

As we look farther and deeper into real-world
Discover at every turn real-world signals encounter physics of practical devices
Thousands of dead physicists are there just waiting for us
Maxwell, Faraday, Lenz, Gauss and all their friends
Say welcome

Real-world systems
Seem filled with black magic
Problems seem to become increasingly mysterious
As signaling frequency increases
If we are to design and build systems for today and tomorrow
That operate reliably and robustly in real-world

We must understand when, where, how, and why
Such physical affects occur

Once we gain such understanding we can
Anticipate impending problems
Potentially can design around or compensate for such problems

Can incorporate such knowledge into our models
To determine and test
✓ How such problems are affecting our system
✓ If our design approach for mitigating affects of real-world
  Has proven successful

Look for the Guilty - A First Look at Signal Quality
In earlier lessons we introduced
Some terminology
Identified and taken a high level view if signaling issues
Move to borders of micro issues and root causes

Will start with basic components
• Resistors
• Capacitors
• Inductors
• Wires - special case of a resistor
Look a DC then AC behaviour

Resistors, Capacitors, Inductors, Wires
Will begin discussion with resistor

Resistor
At the fundamental physical level we have
\[ R = \frac{\rho l}{A} \]
As \( l \) increases / decreases
\( R \) increases / decreases

A increases / decreases
R decreases / increases
Model is ideal - DC model
Key point here – such a model can represent:
- Discrete resistor
- Resistive elements in circuit
- Circuit traces
- Wires

Discrete Component Model
Abstracting one level from physical part
Model in accompanying diagram using *lumped* parameters

At DC or low frequencies
Lumped model considers
All signals appear simultaneously to all interconnected points

At higher frequencies
Must go to *distributed* model
Signals appear at different times to interconnected points

Important questions
- When is modeling important
- Why is modeling important
- When do we move from lumped to distributed model

Using illustrated circuit we can model
✓ Discrete resistor
✓ Wire
✓ Resistive elements in a circuit

Start with high-level view of device behaviour as function of frequency
At DC - We speak of *resistance*
\[ |Z_R(\omega)| = R \quad \omega = 0 \rightarrow \text{no frequency dependent component} \]
\[ |Z_L(\omega)| = \omega L \quad \omega = 0 \rightarrow \text{short} \]
\[ |Z_C(\omega)| = \frac{1}{\omega C} \quad \omega = 0 \rightarrow \text{open} \]
At AC - we now speak of *impedance*
R is resistor - no frequency dependent component
L has finite non-zero impedance
C is finite impedance
\[
|Z_r(\omega)| = R \quad \text{no frequency dependent component}
\]
\[
|Z_L(\omega)| = \omega L \quad \text{finite nonzero impedance – } \omega \text{ increase } \rightarrow \text{ open}
\]
\[
|Z_C(\omega)| = \frac{1}{\omega C} \quad \text{finite nonzero impedance – } \omega \text{ increase } \rightarrow \text{ short}
\]

Impedance as function of S looking into LH port
\[
Z(s) = LS + R \| \frac{1}{CS}
\]
\[
= LS + \frac{R}{RCS + 1}
\]
Let \( S \leftarrow j\omega \)
\[
|Z(\omega)| = \sqrt{R^2(1 - L\omega^2)^2 + (\omega L)^2}
\]

Checking the boundaries
For
\[
\omega = 0,
|z(\omega)| = R
\]
\[
\omega \rightarrow \infty
|Z(\omega)| = L\omega
\]
Observe magnitude of \( Z \)
Beginning to increase again

Because of the inductive and capacitive elements
We also get a phase shift
The value is given by
\[
\phi = \phi_1 - \phi_2
\]
\[
\phi_1 = \tan^{-1}\left(\frac{L}{R \left(1 - L\omega^2\right)}\right)
\]
\[
\phi_2 = \tan^{-1}(RC\omega)
\]
If we now plot $Z(\omega)$ vs frequency for various values of $R$
Get following graphs for $R = 10k$, $1k$, $0.1k$
Observe effect of inductor in each graph

Note
Here down by order of magnitude @ 1GHz
Frequency is 10 GHz

Capacitors
At the fundamental physical level we have

$$C = \frac{\varepsilon A}{d}$$

As $A$ increases / decreases
$C$ increases / decreases
d increases / decreases
$C$ decreases / increases
We have conflicting requirements
Make geometry smaller vs. move components apart

Model is ideal
Like resistor using basic model
Applies to
Discrete components
Parasitic capacitors throughout system
We find parasitic capacitive devices

- Between parallel wires
  - Exacerbated as PCB trace pitch decreases
- Parallel planes
  - Power and ground
    - Here we want the capacitance
- Parallel DC traces
  - Coupling from human bodies

As illustrated we can model

- Parallel printed circuit traces or wires
  - In a printed circuit
    - Two signal traces can form the two plates of a capacitor
      - Here A is small to some extent
- Parallel planes - ground and power planes
  - Here we want it
- Coupling between human bodies and circuit

That capacitor appears as a parasitic device

- Between the two signal traces
  - In accompanying drawing
As we continue to reduce the size of a design

- Those traces are moved closer and closer together
  - The distance between the plates decreases
    - Thereby increasing the associated capacitance

Because the voltage across a capacitor cannot change instantaneously

- Portion of the signal originating at the logic gate on the left
  - Will be coupled into the lower trace as noise
Routing any signal trace through

- Microprocessor, gate array, or programmable logic devices
  - Going to produce the same affect to varying degrees
Discrete Component Model

We model the capacitor as illustrated

As with resistor we’re using lumped parameters
At higher frequencies must go to distributed model

Start with high-level view of device behaviour as function of frequency
At DC
\[ Z_R(\omega) = R \quad \omega = 0 \rightarrow \text{no frequency dependent component} \]
\[ Z_L(\omega) = \omega L \quad \omega = 0 \rightarrow \text{short} \]
\[ Z_C(\omega) = \frac{1}{\omega C} \quad \omega = 0 \rightarrow \text{open} \]

At AC - the capacitor has an impedance
\[ Z_R(\omega) = R \quad \text{no frequency dependent component} \]
\[ Z_L(\omega) = \omega L \quad \text{finite nonzero impedance – } \omega \text{ increase } \rightarrow \text{open} \]
\[ Z_C(\omega) = \frac{1}{\omega C} \quad \text{finite nonzero impedance – } \omega \text{ increase } \rightarrow \text{short} \]

\[ Z(s) = \frac{1}{Cs} + Ls + R \]

Let \( S = j \omega \)

Small at low frequencies
\[ |Z(\omega)| = \left( \frac{(1 - LC\omega^2)^2 + (RC\omega)^2}{(C\omega)^2} \right)^{1/2} \]

Because of the inductive element
We get a phase shift
The value is given by
Equal 0 at low frequencies
\[ \phi = \phi_1 - \phi_2 \]
\[ \phi_1 = \tan^{-1}\left( \frac{RC\omega}{1 - LC\omega^2} \right) \]
\[ \phi_2 = \frac{\pi}{2} \]
If we now plot $Z(\omega)$ vs frequency for various values of $C$

Get following graphs for $C = 1 \mu f, 0.1 \mu f, 0.01 \mu f$

Observe again the effect of the inductor

Inductor
Bogatin, Brooks, Graham and Johnson

A First Look
Inductance and closely related topic of electromagnetic theory
Some of least understood and more challenging of fundamental EE concepts
Play important role in understanding
Real-world effects on electrical signal quality

Have included inductance in models of resistor and capacitor
Now will examine inductance
As specific property / component
How it applies in real-world context

Can base analysis on three fundamental principles
i. There are circular rings of magnetic field lines around all currents
ii. Inductance is number of Webers of field lines around conductor per Amp of current through it
iii. When number of field lines rings around conductor changes
Voltage will be induced across ends of conductor
- Starting with first principle – at the physical level we have
  From Ampere’s Law
  If current flows through a conductor
    Will have magnetic flux field $\Phi$ around the conductor
    Strength of magnetic flux field
      Directly related to magnitude of current flowing
    Direction of flux field
      Found by using right hand rule

  The magnetic field rings
    Always complete circles
    Always enclose some current
    Number of field rings – strength of the field – around a current
      Measured in Webers

  Enclosed current and the effects on magnetic field
    If amount of enclosed current changes
      Find a corresponding change in strength of magnetic field
    Number of Webers of field rings

  Length of conductor affects number of field rings
    Longer wire leads to more rings or flux
  Conductor cross sectional area
    Affects total number of rings surrounding current
  Presence of other nearby currents
    Will affect number of field lines around first current
      Mutual field links first current to the others
    Such an affect can have significant effect on
      Signal quality of first current

- Moving to second principle
  First consider single wire
  Let $I_1$ be driven current

  If $I_1$ changes will cause changing magnetic field
    Changing field will induce a current $I_2$
      In direction to counteract magnetic field that caused it
    Called self-inductance or simply inductance
Initial current $I_1$ causes induced current in opposite direction
Result is zero net flow of current
If change in magnetic field decreases
Induced current $I_2$ decreases thereby increasing net flow of current
In steady state…
No change in $I_1$ →…
No change in magnetic field →…
No induced current →…
No more inductive effect

Formally inductance fundamentally related to
Number of field rings – strength of field – around conductor per Amp of current through it

One Weber / Amp defined as one Henry

Inductance follows directly from Ampere’s Law
Computed as magnitude of magnetic flux per Amp of current
$$ L = \frac{\phi}{I} $$
$L$ – Inductance expressed in Henrys
$\Phi$ – Magnetic flux in Webers
$I$ – Current through conductor in Amps

Now bring a second conductor in close proximity to the first
With no driven current in second conductor
As shown in accompanying diagram
Step 1
Some of the magnetic flux from $I_1$ will induce current $I_2$ in second conductor
Direction of induced current will be such so as to
i. Generate its own magnetic field
ii. That field will counteract magnetic field from $I_1$

Step 2
Flux from the induced current now appears in the second diagram
Some magnetic flux from $I_2$ will couple back to first conductor
Now consider two conductors in close proximity both with driven currents
As in accompanying diagram

Step 1
Some of the magnetic flux from $I_1$ will
Encircle second conductor
Induce current in second conductor

Step 2
Some of the magnetic flux from $I_2$ will
Encircle first conductor
Induce current in first conductor

We see that mutual field lines link the two conductors
Such coupling called *mutual inductance*

- On to the third principle
  Elaborating on the above discussion
  From electromagnetic physics as illustrated in diagrams above
  ✓ DC current through conductor
    Creates constant magnetic field – Oersted’s Law

  ✓ AC or time varying current through conductor
    Creates changing magnetic field
    Measured in Webers
    Induces a voltage in nearby conductors
    Faraday’s Law of Induction

  ✓ AC or time varying current through circuit containing inductance
    Induces voltage opposing change in current – Lenz’s law
    In circuit – *self inductance*
    Nearby circuits – *mutual inductance*
    Like we see above
    If current in conductor changes → magnetic flux changes
    Producing voltage across length of conductor
    Indicated in accompanying diagram

  Voltage induced across wire related to
  Inductance of the wire
  How rapidly current changing
  Will be significant later
Can compute induced voltage as

\[ V = \frac{\Delta \phi}{\Delta t} = \frac{\Delta LI}{\Delta t} = L \frac{dl}{dt} \]

L – Inductance expressed in Henrys
Φ – Magnetic flux in Webers
I – Current through conductor in Amps

As seen above
If second conductor in proximity to first
If we have current in second conductor
Induced or driven
As seen above can have field from second conductor
Going around first

If current in second conductor changes
Resulting change in magnetic flux
Induces voltage in first conductor

Such an induced voltage denoted cross talk or noise

Induced voltage given as

\[ V = \frac{\Delta \phi}{\Delta t} = \frac{\Delta MI}{\Delta t} = M \frac{dl}{dt} \]

M – Mutual inductance expressed in Henrys
Φ – Magnetic flux in Webers
I – Induced current through conductor in Amps

Inductance in Action
Graham and Johnson, Brooks

As noted
Inductance arises whenever there is electric current in conductor
Current creates magnetic field
Energy in magnetic field supplied by driving source

If voltage applied across inductor
Initially no current flow
Current does not change instantly
Magnetic field being created
Builds up over time to steady state value
In accompanying circuit
Voltage step $V_s(t)$ applied
Initially $I(t) = 0$
No current flow $\rightarrow$ output voltage $= V_s(t)$
Result
Initially inductor looks like open circuit

As current build up
Current flow increase $\rightarrow$ decrease in output voltage
Result
In steady state inductor looks like short circuit

Wires and Conductors
Hall, Hall, McCall
Wire or conductor is special case of resistor
Earlier analysis of resistor
Applies to other conductors as well

Recall that the basic discrete resistor model
Analysis
Recognized inductive and capacitive effects
Focused on resistive component

Foregoing analysis will examine inductor in greater detail

From earlier discussion current flowing in conductor
Produces magnetic field and magnetic field leads to inductance
Consider conductor in accompanying diagram
Let current flow into page
Will produce flux as shown
Some of flux will be inside conductor
Some of flux will be outside conductor

Where is the current
Flux density determined by enclosed current
- Flux outside conductor
  Encloses all current flowing through conductor
  Does not depend upon
  Distribution or frequency of current in conductor
• Flux inside conductor
  If current distribution or frequency changes
  Flux distribution will correspondingly change

With DC current moving through the conductor
  Current uniformly distributed throughout body of conductor
  However currents closer to center of conductor will have
    Greater flux density per Amp of current therefore higher self-inductance
    Than those near the outside
  At DC inductive impedance will be zero

With AC current moving through the conductor
  Picture changes – several things come into play
    • Inductive impedance direct function of frequency
      Increasing frequency → increasing impedance
    • Paths with the highest inductance will have highest impedance
    • Current will seek to travel along path with lowest impedance
    • Since center of conductor has highest impedance
      Current will tend to migrate away from center towards periphery

As signaling frequency increases
  Difference in inductive impedance between inner and outer paths increases
  Current distribution changes such that
    Largest density near surface of conductor
    That is current flows mainly in *skin* of conductor
    Such a phenomenon called *skin effect*

Skin is region of conductor between
  Conductor surface
  Internal level called *skin depth*
  Illustrated in accompanying diagram

Such an effect can
  Significantly alter impedance of conductor
  Alter self-inductance to lesser extent

Above analysis tacitly assumes sinusoidal (analog) signaling waveform
  Signal has single frequency
In digital world problem becomes more complex
   Digital signals approximate square waves
       Are wide band signals – contain many frequency components

From Fourier analysis
   Expansion of periodic 50% duty cycle square wave
   \[ f(x) = \sum_{n=1,3,5,...}^{\infty} \frac{1}{n} \sin(2\pi n F x) \]
   \( F \) is frequency
   \( x \) is time

Observe square wave comprises components or harmonics of
   Odd-integer multiples of a fundamental frequency

Each harmonic will see a different inductive impedance
   As it moves along the conductor
   Potentially affecting composite signal quality
   Rise times, fall times, amplitude

Logic Circuits and Parasitic Components
   First Order Models
       Modeling real-world becoming increasingly important
       Note
           For the first order models that follow we cannot have any ringing

Will start by examining the effect of parasitic components
   On the behavior of a logic circuit

Our digital system comprises two logic devices that we model using two buffers
   ➢ Source produces a typical digital signal
       Such as one might find originating from
           Logic gate, a bus driver
       Output of more complex device such as FPGA or microprocessor

   ➢ Receiver of the signal is any similar such device
First Order RC

We’ll begin with a first order model
For the environment and the wire interconnecting the two devices

Use basic logic circuit in following figure for this analysis
Such a model plays a significant role
In first order analyses of typical digital circuit behavior
Results extend naturally to more complex circuits

Now the circuit model

Vin and Vout
Related by simple voltage divider

\[
V_{out}(s) = \left( \frac{1}{Cs} \right) \cdot \left( \frac{1}{R + \frac{1}{Cs}} \right) \cdot V_{in} \\
= \left( \frac{1}{RCs + 1} \right) V_{in}
\]

For Vin a step

\[
V_{out}(s) = \frac{V_{in}}{s} \left( \frac{1}{RCs + 1} \right)
\]

\[
V_{out}(s) = V_{in} \left( \frac{1}{s} - \frac{1}{s + \frac{1}{RC}} \right)
\]
\[ V_{\text{out}}(t) = V_{\text{in}} \left( 1 - e^{-\frac{t}{RC}} \right) \]

**First Order R-L**

Now consider basic R-L circuit

![R-L circuit diagram](image)

Again we compute output as simple voltage divider

\[ V_{\text{out}}(s) = \left( \frac{Ls}{R + Ls} \right) V_{\text{in}}(s) \]

\[ = \frac{s}{s + \frac{R}{L}} V_{\text{in}}(s) \]

For \( V_{\text{in}} \) a step

\[ V_{\text{out}}(s) = \frac{V_{\text{in}}}{s} \left( \frac{s}{s + \frac{R}{L}} \right) \]

\[ V_{\text{out}}(s) = V_{\text{in}}(s) \left( \frac{1}{s + \frac{R}{L}} \right) \]

Which yields

\[ V_{\text{out}}(t) = e^{-\frac{t}{R/L}} \]

Which we plot as
First Order Currents
   Plots of the first order currents
      Will have opposite waveforms

Second Order Series RLC
   ➢ Note
      First order circuits cannot ring whereas second order circuits can
         In real-world such ringing
            Side effect of parasitic inductance and capacitance

Will begin analysis following that for first order circuit
   Use circuit of one signal path in a bus

![Diagram of first-order circuit]

Now extend first-order interconnect model
   By adding parasitic inductance

With addition of inductor
   Now have a second-order circuit
      Diagram shows
         Extended model on left
         Circuit model on right

The modeled capacitor lumps

![Diagram of second-order circuit]

- Package
- Bus
- Outside world
- Ground plane

All add in parallel
Once again we use simple voltage divider to compute $V_{out}$

$$V_{out}(s) = \frac{1}{C_s} \left( \frac{1}{R + Ls + \frac{1}{Cs}} \right) V_{in}(s)$$

$$= \frac{V_{in}(s)}{LC} \left( \frac{1}{\frac{R}{L} s + \frac{1}{LC}} \right)$$

Expression in denominator on right hand side
Can be written as the characteristic equation

Thus

$$V_{out}(s) = \frac{V_{in}(s)}{LC} \left( \frac{1}{s^2 + \frac{R}{L} s + \frac{1}{LC}} \right)$$

$$\omega_n = \frac{1}{\sqrt{LC}}$$

$$\zeta = \frac{R}{2} \left( \frac{L}{C} \right)^{1/2}$$

Recall the value of $\zeta$ determines if circuit is

- Underdamped $\zeta < 1$
- Critically damped $\zeta = 1$
- Overdamped $\zeta > 1$

$$Q = \frac{(L / C)^{1/2}}{R} = \frac{\omega_n L}{R} = \frac{1}{2\zeta}$$
For Vin a step

\[ v(t) = 5 - 5 \exp \left( \frac{-1}{2} \right) \cdot \left( \frac{\sqrt{\frac{4Q^2}{t} - 1}}{Q} \right) \sin \left( \frac{1}{2} \cdot \frac{w}{Q} \cdot t \right) - 5 \exp \left( \frac{-1}{2} \right) \cdot \left( \frac{\sqrt{\frac{4Q^2}{t} - 1}}{Q} \right) \cos \left( \frac{1}{2} \cdot \frac{w}{Q} \cdot t \right) \]

Observe

Sinusoidal behaviour
Exponential envelop

We can plot the behaviour of the circuit as

Tristate Drivers

The tristate driver is commonly used in bus-based applications
To enable multiple different data sources
Onto a system bus

Let’s analyze one signal of such a bus
Examine how the parasitic device can affect performance

The bus signal is presented in accompanying diagram

The capacitor models
Bus, package, and adjacent path parasitic capacitances
This value will be approximately 50pf and
Typical pull-up resistor is 10K for TTLS logic
The parasitic contributions from the interconnecting wire
Do not contribute in this analysis.

When the sending device is enabled and transmitting data
Bus capacitance and wire parasites contribute as discussed earlier
In the circuit in the diagram
Driver has been disabled and is entering the tristate region
We model that turn-off as we did earlier

When the driving device is disabled
The driven bus is now under the control of the pull-up resistor
We model that circuit in the accompanying diagram

If the state of the bus was a logical 0 when the tristate device was disabled
The resistive pull-up voltage acts as a step input into the circuit
The signal, Vout – input to the driven device
Will increase according to the earlier equations
The equation and timing diagram follow our previous analysis

\[ V_{out} = V_{in} \left( 1 - e^{\frac{-t}{RC}} \right) \]

Summary

In this lesson we
✓ Will take some initial steps into the real-world
✓ Examined a high-level view of and lay foundation for study of digital signaling and signal quality
✓ Introduced some related concepts and vocabulary
✓ Introduced and examine basic issues affecting digital signal quality
✓ Moved into advanced area called signal integrity