FPGAs & Multi-FPGA Systems

Fit logic into a prefabricated system
Fixed inter-chip routing
Fixed on-chip logic & routing

FPGA Abstract Model

Logic cells imbedded in a general routing structure

Logic cells usually contain:
- 6-input Boolean function calculator
- Flip-flop (1-bit memory)

All features electronically (re)programmable
Real FPGA Architecture – Altera Stratix V

Note: Most pictures following courtesy of Mike Hutton/Altera Inc.

Altera Stratix V Device Floorplan
The k-Input LUT (e.g. k=4)

\[ a'b'c'd' + abcd + abc'd' = 1000 0000 0000 1001 = 0x8009 \]

Adaptive Logic Module
Stratix V ALM

Stratix V ALM Modes
LAB Interface

Hierarchy: LAB / Cluster
Memory in Stratix Devices

MLABs
- Change LABs into dual port memories
  - 10x32 addr by 2bit
  - 10x64 addr by 1bit

- FIFO Buffers
- Shift Registers
- Delay Lines
- Small ROMs

M20K Blocks
- 20Kbit on-chip blocks
dual port w/ parity
  - 16K addr by 1bit
  - 8K addr by 2bit
  - 512 addr by 32bit
- Large on-chip storage
- Intermediate results
- Caching & data reuse

External Memory
- DRAM, SRAM, & FLASH interfaces
- Multiple Gbytes

- Huge Datasets
- Longer-term storage

More Bits for Larger Memory Buffering

More Data Ports for Greater Memory Bandwidth
DSP Blocks (18-bit mode)

DSP Blocks (High-precision mode)
## Putting it all Together

![Diagram of Stratix V](image)

### Logic
- ALMs (4xReg, 4xLUT, ...): 172K
- DFFs: 690K
- 4-LUTs: 690K
- Hard Multipliers: 3,180 (18x18), 1,590 (27x27)

### Memory
- 64x10b MLABs (uses ALMs): 4.3K (344KBytes)
- M20K blocks: 2,014 (4.9MBytes)

### I/O, Clocks
- PCIe hard IP blocks: 1
- DDR3 Interfaces: 4
- 14.1Gbps transceivers: 24
- Clock Generators (PLLs): 24

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## Stratix V Statistics (5SGSD5H2F35I3LN)

<table>
<thead>
<tr>
<th>Category</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
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<td></td>
</tr>
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FPGA Roles

- Digital logic implementation & prototyping
- Multi-mode systems
  - Change functionality for different applications
- Logic emulation
- Stream-based computing
- Processor acceleration

Partitioning

For Multi-FPGA System:
- Break logic into individual FPGAs
- Respect inter-FPGA communications
- Similar to placement

Techniques
- Multi-level partitioning (xbars)
- Simulated Annealing
Virtual Wires

Multi-FPGA systems typically pin-limited, not logic limited

FPGA: up to 1 Million logic gates, 512 I/Os.
Partitioned circuit components might be:
10x(1 Million gates, 5,000 I/Os)
100x(100,000 gates, 500 I/Os)

Solution:
20x(1/2 Million gates, 2,500 I/Os + time division multiplexing on I/Os)

Global (Inter-FPGA) Routing

Route from source to destination FPGA using fixed resources
Similar to Aphyds Global Routing, but with fixed capacities
Maze, Steiner, etc. all can be applied
Must deal with potentially non-geometric distances
**Technology Mapping**

Take circuit and map it into the basic elements of the FPGA
5-LUTs
Must consider multiple factors
  logic decomposition
  logic replication
  reconvergent fanout

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**Placement**

Assign logic blocks to specific chip locations
Virtually identical to Aphyds Placement
Seek to minimize routing distance, congestion
FPGA Routing

Must pick the individual resources to use to carry a signal
fixed capacity
potentially non-geometric distances
balance demands of multiple routes

Pathfinder (McMurchie, Ebeling)
Convert routing architecture to graph
Ignore congestion – change penalties and iterate
Use maze + A* routing
Integrate performance and congestion avoidance into one algorithm

Pathfinder

Represent all interconnection resources as a directed graph
Pin permutations on LUT inputs also captured

Routing sketch:
Each iteration rip-up and reroute all signals independently.
Resources currently used by another net cost more
Between iterations increase cost of resources that are shared

-> Over time, signals “bid” on preferred route, negotiating a compromise
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CAD & Physical Design

CAD = Computer Aided Design

Complexity of today’s circuits requires computer support for most design tasks

CAD split into Synthesis, Physical Design

Synthesis = translating designer requirements into a circuit graph

PD = translating circuit graph into layout ("blueprint") for fabrication